## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A data transfer circuit for latching an input data in a first latch section, transferring a first latch result of said first latch section to a second latch section, and latching said first latch result in said second latch section, characterized by:

transferring only an inverted output of said first latch result to said second latch section ~~or transferring only a non-inverted output of said first latch result to said second latch section~~; and

raising a power supply voltage of said first latch section from a first voltage to a second voltage while said first latch result is transferred to said second latch section;

wherein said second voltage is higher than said first voltage, and

wherein said second voltage is a power supply voltage of said second latching section.

2. (Withdrawn) A flat display apparatus that sequentially inputs gradation data indicative of brightness of each pixel and displays an image based on said gradation data in a predetermined display section, said flat display apparatus characterized by having:

a plurality of latch circuits for sampling said gradation data sequentially and cyclically, and distributing said gradation data to a corresponding line; and

a digital/analog conversion circuit for setting an output signal level to said corresponding line depending on a latch result of said latch circuits, in which each of said plurality of latch circuits is characterized by:

latching said gradation data in a first latch section at a respective timing corresponding thereto, data transferring a latch result of said first latch section to a second

latch section simultaneously and in parallel in said plurality of latch circuits to output the result to said digital/analog conversion circuit;

data transferring only an inverted output of the latch result of said first latch section or only a non-inverted output of the latch result of said first latch section to said second latch section; and

raising a power supply voltage of said first latch section at least during a period of data transfer of the latch result of said first latch section to said second latch section.

3. (Currently Amended) The data transfer circuit according to claim 1, wherein said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to a transfer of said first latch to said second latch section by only an inverted output ~~or only a non-inverted output~~.

4. (New) A data transfer circuit comprising:

a first latch section that latches a data input and produces a first latch result; and

a second latch section that latches said first latch result and outputs a transfer circuit output;

wherein the first latch result is transferred to the second latch section by use of a single phase,

wherein a power supply voltage of said first latch section is raised from a first voltage to a second voltage while said first latch result is transferred to said second latch section, and

wherein said second voltage is higher than said first voltage, and said second voltage is a power supply voltage of said second latching section.

5. (New) The data transfer circuit according to claim 4, wherein said transfer by use of a single phase is carried out by use of an inverted output of the first latch result.

6. (Withdrawn – New) The data transfer circuit according to claim 4, wherein said transfer by use of a single phase is carried out by use of a non-inverted output of the first latch result.

7. (New) The data transfer circuit according to claims 4, wherein said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to the transfer of said first latch result to said second latch section.

8. (New) The data transfer circuit according to claims 5, wherein said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to the transfer of said first latch result to said second latch section.

9. (Withdrawn – New) The data transfer circuit according to claim 6, wherein said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to the transfer of said first latch result to said second latch section.

10. (New) The data transfer circuit according to claim 4, wherein said data input is gradation data.

11. (New) The data transfer circuit according to claims 5, wherein said first latch section further comprises a first inverter and a second inverted, said first and second inverters arranged in parallel between said power supply voltage and a first negative power supply;

wherein said data input is inputted to said first inverter.

12. (New) The data transfer circuit according to claim 11, wherein an output from said first inverter is inputted to said second inverter via a switching circuit that operates off-action at a sampling pulse.

13. (New) The data transfer circuit according to claim 12, wherein said data input is inputted to said first inverter via a transistor which operates on-action at said sampling pulse.

14. (New) The data transfer circuit according to claim 5, wherein a transfer switch is arranged between said first latch section and said second latch section, an output of said transfer switch being supplied to said second latch section.

15. (New) The data transfer circuit according to claim 5, where in said second latch section further comprises a third inverter and a fourth inverted, said third and fourth inverters arranged in parallel between said power supply voltage maintained at said second voltage and a second negative power supply;

wherein said first latch result is inputted to said third inverter and the output of said third inverter is inputted to said fourth inverter.

16. (New) The data transfer circuit according to claim 14, wherein said second latch section level shifts said transfer circuit output by setting-up said second negative power supply.